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**APPLICATION
FOR
UNITED STATES
LETTERS PATENT**

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**FOR: SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD THEREOF**

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SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a semiconductor device and a manufacturing method thereof and more particularly to an improvement on a SOC (System On Chip) that has a logic (logic circuit) and a DRAM (Dynamic Random Access Memory) together on one and the same substrate.

10 2. Description of the Related Art

 In a general purpose DRAM (having, on one chip, only a memory section and an adjacent circuit section which comprises a decoder, a sense amplifier, an I/O (input/output) circuit and the like), hold characteristics of memory cells have been, 15 hitherto, regarded as the matter of great importance so that it has become a common practice to set the dopant concentration in the source-drain regions of cell transistors lower than that in the adjacent circuit section for the purpose of achieving the suppression of the junction leakage current.

20 Meanwhile, in recent years, demands that image processing using computer graphics should be made at a higher speed have been growing. Accordingly, there has been proposed a DRAM-incorporated logic chip as shown in Fig. 9, a so-called

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SOC 31 which has a DRAM section 32 comprising memory cells 33 and adjacent circuits 34 such as a decoder and a sense amplifier, a logical operation section (a logic section) 35 where graphic processing is carried out at a high speed, and, in addition, an I/O section 36 which connects these DRAM and logic sections with an external circuit, all together on one chip.

In the DRAM section thereof, to suppress the short channel effect and relax the centralization of the drain field, the dopant concentration in the source-drain (S/D) should be, hitherto, set low. This makes the junction in the S/D regions shallow and, as has been pointed out, the silicidation therein may bring about an increase in the leakage current. In light of this problem, several techniques of making silicidation in the DRAM section have been proposed

For example, Japanese Patent Application Laid-open No. 97649/1999 discloses the methods using the following SOC structures: that is, (1) a structure (first embodiment) wherein, while the dopant concentration in S/D regions of a memory cell region in a DRAM section is set low to make the leakage small, dopants are implanted into S/D regions of an adjacent circuit region to a high concentration, and besides silicide layers are formed on gate surfaces and the surfaces of active regions, and thereby high-speed operations become

002260-9079960

attainable; (2) a structure (second embodiment) wherein, in a DRAM cell section, S/D regions (low dopant-concentration regions) with which capacitor contacts are connected are set as non-silicide regions, and silicide layers are formed only on the surfaces of S/D regions (low dopant-concentration regions) with which bit line contacts are connected and on the gate surfaces of cell transistors, whereby the interconnection resistance and the contact resistance are reduced, and reading and writing operations at a higher speed are made attainable; and (3) a structure (third embodiment) wherein, in a DRAM memory cell section, portions of a TEOS (Tetra-Ethyl-Ortho-Silicate) oxide film that is first laid at the time of formation of transistor sidewalls are selectively left at the edge of LOCOS (Local Oxidation of Silicon), or in the vicinity of bird's beaks, and thereafter silicide layers are formed on the entire surface of the DRAM memory cell section but said portions, in the same way as for cell gates and a logic section, and thereby reading and writing operations at a higher speed are made attainable, while the junction leakage is kept low. As an example, the third embodiment in said publication is now described in detail with reference to a schematic cross-sectional view of a memory cell section shown in Fig. 10. A semiconductor substrate 41 is isolated into elements by isolation oxide films 42 and a memory

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cell transistor is formed between these films. Silicide layers 49 are formed on the surfaces of the gate electrodes 48 and in regions where a contact 52a connecting with a bit line 51 and contacts 52b connecting with storage nodes 53 are in contact with the semiconductor substrate 41, respectively. These silicide layers lying on the substrate are formed within low dopant-concentration regions 47. At the edge sections of the isolation oxide films 42, there are formed TEOS oxide films 50, protecting these edge sections from silicidation, so that silicide layers may not be formed beneath the isolation oxide films 42 or the junction leakage may not be generated around the edges thereof. In the drawing, 43-45 each represents an interlayer insulating film; 46, gate oxide films; 54, a dielectric film and 55, a cell plate.

Further, Japanese Patent Application Laid-open No.17129/1999 discloses a structure wherein, after S/D regions of transistors in a DRAM cell section and a logic section are formed in separate steps, respectively, and contact-holes that reach S/D regions of transistors for cell selection are formed, silicide layers are formed on the surfaces of the S/D regions through said contact-holes so that conductive films are buried in the contact-holes. In this instance, silicide layers are also formed in the S/D regions of transistors in the logic section but this silicidation is

carried out in a different step from the one for silicidation of the S/D regions of transistors for cell selection. Further, it is therein mentioned that silicidation can be also applied to the gate surfaces in another step.

5 In any of these conventional techniques, the S/D regions of DRAM cell transistors are still formed to have a low dopant concentration, while the S/D regions of transistors in the logic section, a high dopant concentration. In other words, a SOC structure of this sort is designed under the concept
10 that a high-speed logic is made incorporated into an existing DRAM. This assumes fabrication of the DRAM section and the logic section in separate steps and, thus, a reduction of the production cost cannot be much expected to happen. However, the SOC is, by nature, designed and manufactured for each
15 system application. In comparison with the general purpose DRAM, a small quantity and a large diversity characterize its production, and, therefore, the cost reduction has a particular significance.

SUMMARY OF THE INVENTION

20 An object of the present invention is, therefore, with such a pre-concept relinquished, to provide a manufacturing method that can produce, with low cost, an SOC having necessary and sufficient characteristics in the DRAM section, while

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attaining higher-speed performance of the whole elements therein, on the basis of a novel concept that a DRAM is made incorporated into a high-speed logic, and a structure of the SOC thereat.

5 Accordingly, the present invention relates to a
DRAM-incorporated semiconductor device which has a DRAM
section and a logic section being formed on one and the same
substrate, wherein silicide layers are formed, at least, on
all the surfaces of the source-drain regions and the gate
10 surfaces of transistors in the DRAM section and the logic
section. Further, the present invention relates to a method
of manufacturing a DRAM-incorporated semiconductor device in
which a DRAM section and a logic section are formed on a
semiconductor substrate that is isolated into elements,
15 wherein silicidation of all the surfaces of the source-drain
regions and the gate surfaces that constitute transistors in
the DRAM section and the logic section is carried out
concurrently in one and the same step.

 Further, the present invention relates to a
20 semiconductor device having a memory cell section and an
adjacent circuit section, wherein silicide layers are formed
on all the surfaces of the source-drain regions and the gate
surfaces of transistors in the memory cell section and the
adjacent circuit section.

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In the present invention, the source-drain regions in the DRAM section are made high dopant-concentration regions and consequently, through silicidation of all the surfaces of said regions and the gate surfaces, good ohmic contacts can be formed. Further, the formation of silicide can be carried out concurrently with silicidation in the logic section in one and the same step. Therefore, an increase in the number of the steps in a manufacturing method can be avoided, and both higher-speed performance of the whole elements and lower cost production can be realized.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-8 are a series of schematic cross-sectional views illustrating the steps of a manufacturing method of a semiconductor device that is one embodiment of the present invention.

Fig. 9 is a schematic view showing an example of the structure of a SOC having a DRAM on board.

Fig. 10 is a cross-sectional view showing a conventional DRAM cell section.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, the present invention is described in detail below. Figs. 1-8 are a series of schematic

cross-sectional views illustrating the steps of a manufacturing method of a semiconductor device that is one embodiment of the present invention.

First, onto a Si substrate 1, buried oxide films 2 are
5 formed by the known method of trench isolation so as to isolate
an N-MOS (N-Metal-Oxide-Semiconductor) and a P-MOS of a logic
section and a DRAM section each as an element. Next, over the
surface of the substrate 1, a thin oxide film (a SiO_2 : sacrifice
oxide film, not shown in the drawing) is formed by thermal
10 oxidation, and then the channel ion implantation for forming
P-channels and N-channels to the logic section and adjacent
circuits which comprise a decoder and a sense amplifier in
the DRAM section, an I/O circuit and the like, and forming
N-channels to memory cells, together with the ion implantation
15 for forming respective wells (a P-well 3, an N-well 4 and a
cell P-well 5) are performed. This accomplishes formation of
the structure shown in Fig. 1. Although Fig. 1 shows, for the
sake of simplification, only respective wells, buried oxide
films 2 for element isolation and a memory cell in the DRAM
20 section, it is apparent that the present invention is not
limited to this structure. Further, the ion implantation for
the cell P-well 5 and the P-well 3 may be performed
simultaneously or separately. A deep N-well may be
additionally formed in the memory cell region.

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After removing the sacrifice oxide film, a gate oxide film (not shown in the drawing) is formed by another thermal oxidation. Hereat, it is preferable to make the gate oxide film thicker in the DRAM section than in the logic section.

5 A polysilicon layer that is to serve as respective gates of all transistors is, then, formed over the entire surface and patterned into a prescribed shape of gate electrodes. After that, dopant ions are implanted thereinto so as to form LDD (Lightly-Doped Drain) regions 7a, 7b and 7c, in respective
10 sections. Formation of the LDD regions 7a and 7c may be performed, hereat, simultaneously or separately.

Subsequently, using TEOS or the like, an oxide film is grown over the entire surface by the CVD (Chemical Vapour Deposition) method and, through anisotropic etching, LDD sidewalls 8 are
15 formed on lateral faces of gate electrodes (Fig. 2).

Next, as shown in Fig. 3, masking the N-MOS section and the DRAM section with a resist 9a, only the P-MOS section is left exposed, and p-type dopants such as B or BF_2 are ion-implanted for formation of the S/D regions 10a in the P-MOS
20 section. For example, BF_2 is ion-implanted under the conditions that the accelerating voltage is 20 keV and the dose is $3\text{E}15$ or so. Hereat, the gate polysilicon is also subjected to the ion implantation simultaneously and, as a result, becomes a P-gate.

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Next, as shown in Fig. 4, a resist 9b is formed only in the P-MOS section, and n-type dopants such as P or As are ion-implanted into the N-MOS section and the DRAM section, for example, As is ion-implanted at 50 keV to a dose of 3×10^{15} to 6×10^{15} or so, thus forming S/D regions 10b and 10c, respectively. Hereat, the gate polysilicons are also subjected to the ion implantation simultaneously and, as a result, become N-gates. In effect, there are formed so-called P-N gates in which the P-ch has a P-gate and the N-ch, an N-gate. After that, for example, the RTA (Rapid Thermal Annealing) (ramp annealing) is performed at 1000 °C for 10 seconds or so, and the implanted dopants are activated. While ion-implantation is, hereat, applied to the N-MOS section and the DRAM section at the same time, it can be applied to each in separate steps.

Next, as shown in Fig. 5, a metal film for silicidation is grown over the entire surface by the sputtering method or the like. Here, an example in which a cobalt (Co) film 11 is grown is shown. However, the present invention is not limited to this and any metal material that can form silicide through a thermal reaction with silicon, such as titanium and nickel, can be utilized in the same manner.

Next, the unreacted Co film 11 is removed by a heat treatment. For example, a heat treatment in N_2 gas atmosphere at a temperature of 500-600 °C or so is applied thereto for

002260-9079960

30 seconds and then the unreacted Co film is removed with a
mixed solution of sulfuric acid and hydrogen peroxide, and
another heat treatment in the nitrogen gas atmosphere at 800
°C is further applied thereto for 10 seconds or so (the
5 so-called salicide method), which results in formation of
cobalt silicide (CoSi_2) 12 over all the surfaces of the S/D
regions (10) and on the gate electrodes (6), as shown in Fig.
6.

Subsequently, in the same way as the prior art, a first
10 interlayer film 13 is formed and thereafter contact holes to
connect to capacitor electrodes are formed in the DRAM section,
and then, by filling up the contact holes with a metal or a
polysilicon, capacitor contacts 14 are formed. Lower
electrodes 15, capacitor insulating films which are omitted
15 from the drawing and upper electrodes 16 are then formed to
accomplish capacitor electrodes (Fig. 7). Although
stacked-type capacitor electrodes are, herein, shown as lower
electrodes, the present invention is, in no way, limited by
this, and can have known cylindrical electrodes or electrodes
20 with an even more complicated structure for them. When
utilizing polysilicon, HSG (Hemispherical Silicon Grain)
electrodes can be also employed. Further, the capacitor
contacts, lower electrodes and upper electrodes may be formed,
using a known material such as Ti/TiN/W or the like. In short,

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the material, the structure and such can be selected appropriately for them according to design.

Following this, as shown in Fig. 8, after a second interlayer film 17 is formed, contacts 18 each connecting with one region of the S/D regions of transistors in the logic section and a bit line contact 19 connecting with the DRAM section are formed, using a known metal material such as Ti/TiN/W or the like. Next, a known interconnection material such as Al, TiN, W or the like is grown over the entire surface by the sputtering method and then patterned, whereby a first interconnection 20 that is also to serve as a bit line is formed. Obviously, the bit line and the first interconnection can be formed as different layers or from different materials.

Further, when forming contact holes, it is preferable to form an etching stopper layer on the substrate so that the pre-formed silicide layers may not be carved into at the time of etching.

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20 What distinguishes the present invention from the conventional techniques the most is the fact that, even in the memory cell region of the DRAM section, there are formed the S/D regions with a high dopant concentration defined as n^+ . When silicide is formed on the S/D regions with such a high dopant concentration, good ohmic contacts can be formed. Further, because the junction becomes deeper, the junction

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leakage current is hardly generated even if silicide is formed over all the surfaces of the S/D regions. In contrast with this, when silicide is formed on conventional low dopant-concentration regions (N⁺), Schottky contacts are formed therebetween, which is not adequate for the purpose of achieving lower resistance.

Further, by setting the S/D regions of the memory cell regions as high dopant-concentration regions, good ohmic contacts can be formed through silicidation, as described above, so that this invention can be readily put into practice. Moreover, as the present invention has a considerable effect of making the performance of the whole elements faster and the steps of a manufacturing method simpler, its technical significance cannot be overemphasized.

While, for the above description, a DRAM-incorporated SOC is given as an example, the present invention can be applied to a semiconductor device that does not have any logic section, that is, a semiconductor device having only a DRAM section. Further, the present invention can be applied to a semiconductor device having a DRAM cell section and an adjacent-circuit-functional element section, wherein silicide layers are formed over all the surfaces of the source-drain regions and the gate surfaces of transistors in the DRAM cell section and the adjacent-circuit-functional

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element section which comprises elements such as various decoders, sense amplifiers and the like. In this instance, too, silicidation of the DRAM cell section and the adjacent circuit section can be carried out concurrently in one and
5 the same step, in accordance with the above description, and thereby both higher-speed performance of the whole elements and simplification of the manufacturing steps can be attained.

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